PROTEUS
Flip-flops

Dr Diarmuid Ó Briain

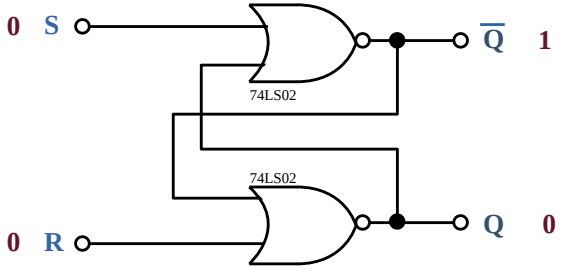
Learning objectives

- Getting started with Proteus design Suite ✓
- First PROTEUS 8 Schematic ✓
- LED & Switch animation ✓
- Digital to Analogue Conversion ✓
- Logic Gates ✓
- Digital Logic ✓
- **Digital logic, Flip-Flops**
- Analogue Signals
- Graphs

Set – Reset Flipflop (SR)

- The SR flip flop is a 1-bit memory bistable device having two inputs
  - SET
  - RESET
- The reset input is used to return the flip flop to its original state from the current state with an output 'Q'.

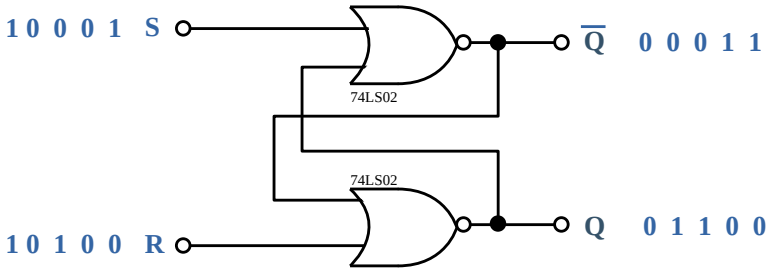
SR Flip-flop - Cross-coupled NOR gates



INPUTS		OUTPUTS	
S	R	Q	$\overline{Q}$
1	0		
0	0		
0	1		
0	0		
1	1		

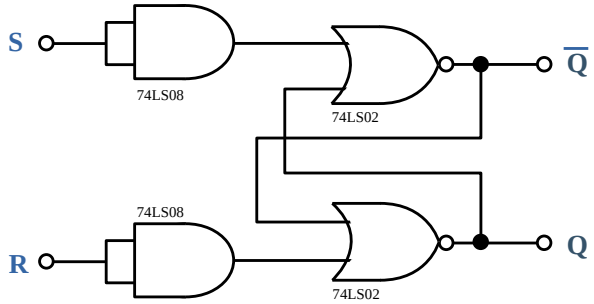
- Fill out truth table.

SR Flip-flop - Cross-coupled NOR gates



INPUTS		OUTPUTS		
S	R	Q	$\overline{Q}$	
1	0	1	0	
0	0	1	0	[after S=1, R=0]
0	1	0	1	
0	0	0	1	[after S=0, R=1]
1	1	0	0	[Unstable state]

SR Flip-flop laboratory

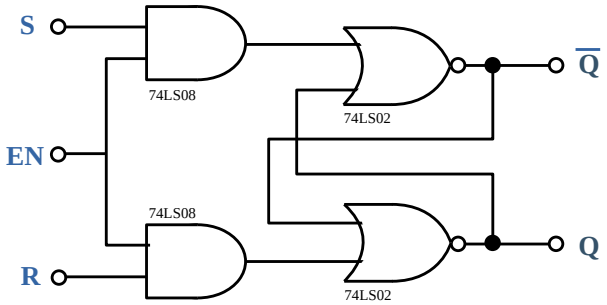


- Consider the following, is it different from the previous circuit?

Gated SR Flip-flop

- A **gate** (**EN**) input is added to the SR flip-flop to make the flip-flop synchronous.
- For the **SET** and **RESET** inputs to change the flip-flop, the gate input must be active (**high**).
- When the gate input is **low**, the flip-flop remains in the hold condition.

Gated SR Flip-flop

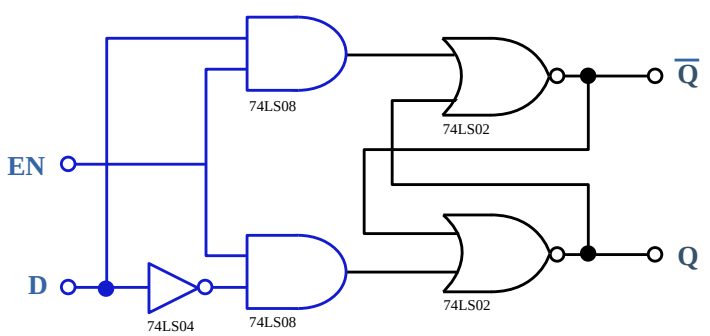


Laboratory #2

D-latch Flip-flop

Gated Delay (D) latch Flip-flop

- Exploits the fact that, in the two active input combinations (01 and 10) of a gated SR latch, R is the complement of S.
- A gated D-latch may be considered as a one-input synchronous SR latch.



JK Flip-flop

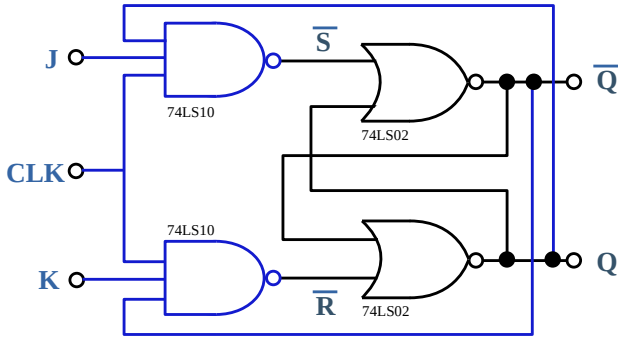
- The basic SR flip-flop circuit suffers from two basic switching problems.
  - The **SET = 0** and **RESET = 0** condition (**S = R = 0**) must always be avoided
  - If **SET** or **RESET** change state while the ENable (**EN**) input is **high** the correct latching action **MAY NOT** occur
- The **JK** flip Flop is considered to be a universal flip-flop circuit.
- The two inputs labelled **J** and **K** are not shortened abbreviated letters just picked to differentiate from other letters.

JK Flip-flop

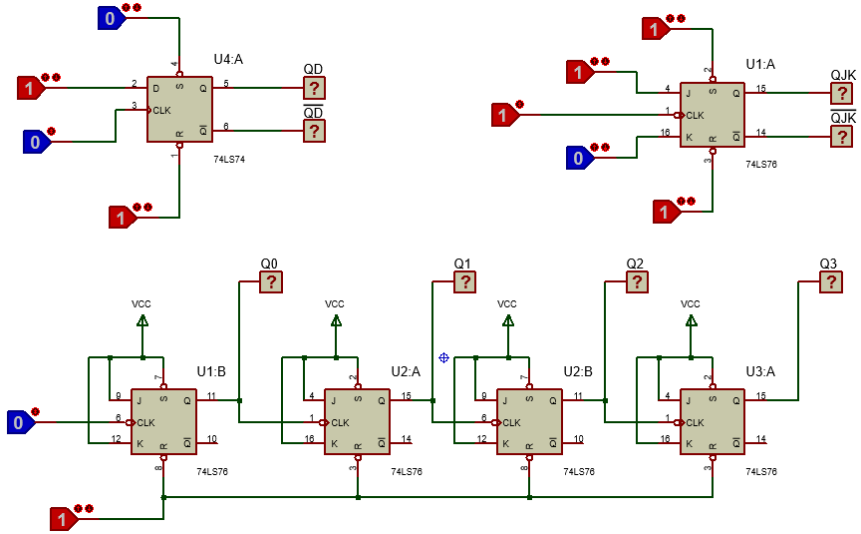
- The **JK** flip flop is essentially a gated SR flip-flop with the addition of a clock input circuitry that prevents the illegal or invalid output condition that can occur when both inputs **S** and **R** are **high**.
- JK flip-flop has four possible input combinations,
  - High (1)
  - Low (0)
  - No change
  - Toggle.

JK Flip-flop

- The JK flip-flop augments the behaviour of the SR flip-flop (J: Set, K: Reset).
  - J = K = 1 = Toggle
  - J = 1, K = 0 = SET
  - J = 0, K = 1 = RESET



D and JK Flip-flop Laboratory



Learning objectives

- Getting started with Proteus design Suite ✓
- First PROTEUS 8 Schematic ✓
- LED & Switch animation ✓
- Digital to Analogue Conversion ✓
- Logic Gates ✓
- Digital Logic ✓
- Digital logic, Flip-Flops ✓
- Analogue Signals
- Graphs

Bóthar Chill Chainnigh, Ceatharlach
Suiomh Gréasáin: www.itcarlow.ie
Guthán: (059) 917 5000
R-phost: diarmuid.obriain@itcarlow.ie

INSTITUTE of TECHNOLOGY CARLOW
Institiúid Teicneolaíochta Cheatharlach

EUR ING Dr Diarmuid Ó Briain
Innealtóir Cairte

Léachtóir

Athena SWAN Bronze Award
GENDER CHARTER
CYBER IRELAND

engcore
advancing technology